Chip - Fabrication

Everything starts with sand...

SiO₂ + 2C $\rightarrow$ Si + 2 CO

SiO₂ quartz sand
2C carbon
2000 °C Si silicon purity: 97%
but we need: 99.99999%

Hyper pure polysilicon production

1. Hydrochlorination of Silicon
   Si + 3 HCL $\rightarrow$ SiHCL₃ + H₂

2. Distillation of Trichlorosilane, impurities such as Fe, Al and B are removed, impurities < 1 ppm/cm³

3. Reduction back to Silicon
   SiHCl₃ + H₂ $\rightarrow$ Si + 3 HCl

After this chemical process, the polycrystalline silicon must be transformed into ingots with a singular crystal orientation.
Czochralski-Process

Poly-Si chunks are loaded into the crucible.

For p-type wafers we put Boron into the crucible, for n-type wafers Phosphorus.

If the poly-Si is melt, a "seed" of single crystal silicon is putted into the melt.

The ingot grows with the same crystal orientation.

Ingot

Ingots coming from crystal growing are slightly oversized in diameter and typically not round.

With a grinding wheel the ingot is shaped to a precision needed for wafer.

Round Grinding Process
Wafer Slicing

Multi-Wire Slicing

Ingots are sliced into wafers with a thickness of about 0.8mm.
Diameter of the cutting wire: ~0.15mm
Cutting speed: ~2cm/h

Edge Contour Grinding

edges of as-cut wafers are sharp and need to be shaped to make the wafer robust against further handling and mechanical stress.

Lapping

Wire sawing does not produce perfectly flat wafers, so lapping is necessary.
Lapping removes variations of thickness.

Lapping
Wafer Etching

After lapping, the wafer is very flat, but the surface is rough. Furthermore on the top of the wafer, there is a layer where the orientation of the atoms is heavily disturbed. These damaged layers are removed in a chemical etching procedure.

Polishing process

Perfecting the wafer surface

Gives the surface the required atomic flatness

Extremely particle sensitive → clean room environment necessary

Laser Inspection

Lasers scan the wafer surface for surviving particles and defects

If the laser detects imperfections, the light is irregularly reflected from the wafer surface

Requirements: no particles or defects greater than 0.3 microns

Blank Wafer

Different wafer sizes:
- 3” (76mm)
- 4” (100mm)
- 5” (125mm)
- 6” (150mm)
- 8” (200mm)
- 12” (300mm) Pizza-Wafer

Different wafer types:
- p-type wafer (boron)
- n-type wafer (phosphorus)

Costs for a 200mm Si-Wafer: 80 €
Completed Wafer

processing line

Sand
Silicon Ingot
Blank Wafer

Packaged die
Individual dice
Patterned Wafer

Oxidation

2 methods
- Dry Oxidation: Si + O₂ → SiO₂
  - used for thin oxide (gate oxide)
- Wet Oxidation: Si + 2H₂O → SiO₂ + 2H₂
  - used for thick oxide (field oxide for isolation)
  - 44% of the oxide layer grows into the substrate, 56% grow on top of the Si.
  - Loading wafers into oxidation furnace (temperature ca. 1200°C)
  - Oxide thickness of 1µm:
    - dry: 25 hours
    - wet: 75 min

LOCOS

LOCAL Oxidation of Silicon

- Oxide grows at those parts of the wafer surface where no Si₃N₄ covers the wafer
- Used for isolation between transistors
- Limited structures because of bird’s beak
Ion Implantation

- Ion implantation has been best equated with firing a machine gun into a wall. In this analogy the wall is the wafer and the bullets are the ions.
- Atoms are ionized, accelerated in an electric field and implanted into the target material.
- Short process times, good homogeneity, exact control of the amount of implanted ions, different materials can be used for masking.

Resist Spin

- Photo resist is applied to the wafer by spinning it onto the wafer surface using a spin coater.
- Typical duration: 15 - 30 sec at 3000 - 6000 rpm.

Lithographic Process

1. Cover whole surface with photo resist.
2. UV-light goes through a mask and exposes the photo resist. Photo resist becomes soluble.
3. The wafer is developed in acid or base solution to remove the exposed photo resist.
4. Material is removed from areas that are not covered by photo resist using acids, bases and caustic solutions. Processing steps (e.g. ion implantation) can be applied now.
5. The remaining photo resist is removed.

Lithography
CMOS Process

N-well creation (1/2)

- base material is p-substrate wafer
- deposit SiO₂ (silicon dioxide), Si₃N₄ (silicon nitride), and photo resist on Si-wafer
- expose photo resist with UV-light through the N-WELL mask

CMOS Process

N-well creation (2/2)

- remove exposed photo resist
- etch Si₃N₄ and SiO₂
- create n-well for fabrication of p-channel devices via ion-implantation with Phosphorous
- remove remaining resist
- etch Si₃N₄ and SiO₂

⇒ N-well created

CMOS Process

Isolation between the transistors (1/2)

- deposit SiO₂ (silicon dioxide), Si₃N₄ (silicon nitride), and photo resist
- expose photo resist through the ACTIVE-mask
- remove exposed photo resist

CMOS Process

Isolation between the transistors (2/2)

- etch Si₃N₄ and SiO₂
- remove remaining resist
- Local Oxidation Of Silicon (LOCOS): a thick field oxide grows where the Si-wafer isn’t covered with Si₃N₄
- etch Si₃N₄

⇒ isolation between n-channel and p-channel created
CMOS Process produce Poly-Silicon gates (1/2)

- deposit Poly-Si and photo resist
- expose photo resist through the GATE-mask

CMOS Process produce Poly-Silicon gates (2/2)

- remove exposed photo resist
- etch Poly-Si
- remove remaining resist

CMOS Process produce source and drain areas of n-channel devices

- deposit photo resist
- expose photo resist through the n+ mask
- remove exposed photo resist
- create source and drain via ion-implantation with Arsenic (self aligned by Poly-Si gate)
- The Poly-Si gate acts like a barrier for this implant to protect the channel region.
- remove remaining resist

CMOS Process produce source and drain areas of p-channel devices

- deposit photo resist
- expose photo resist through the p+ mask
- remove exposed photo resist
- create source and drain via ion-implantation with Boron (self aligned by Poly-Si gate)
- The Poly-Si gate acts like a barrier for this implant to protect the channel region.
- remove remaining resist

S and D of nMOS created

S and D of pMOS created
CMOS Process

Contacts creation

- deposit SiO₂ and photo resist
- expose photo resist through the CONTACT mask
- remove exposed photo resist
- etch SiO₂
  \[ \text{contact holes created} \]

Metallization

- deposit photo resist
- expose photo resist through the METAL mask
- remove exposed photo resist
- etch SiO₂
- remove remaining resist

CMOS Process

Metallization & Passivation

- A thin layer of aluminum (or copper) is evaporated or sputtered onto the wafer.
- CMP (Chemical Mechanical Planarization) to get a plane surface
- deposit Si₃N₄ for surface protection
  \[ \text{CMOS Process finished} \]

more metal layers can be created with the help of the lithographic steps
**Wafer Stepper**

- Wafer is fixed on a moveable device in x and y direction.
- Light goes through the mask, lens, and the objective.
- The structures from the mask are mapped to the wafer.

**The Mask (Reticle)**

- There are special structures in the mask to focus the light of the wafer stepper.
- Mask contains some chips.

**The Stepping Process**

- The mask may contain structures of more chips used for: MPW-runs.
- The structure is mapped to the wafer in the sequence shown by the red arrows.

**The Wafer after the process**
**Wafer Test**

**In-line Parametric Test (DC test):**
- done on test structures located on the wafer.
- In-line parametric data is collected on a sample basis and interpreted by engineers to improve the fabrication process.
- test will identify process problems

**Wafer Sort:**
- at the end of the fabrication each die is electrically tested
- functional test
- ink faulty dice

Wafer test is the measurement of electrical parameters on ICs at the wafer level to verify conformance to specifications.

**Dicing (cutting the wafer):**
- wafer is fixed with blue tape
- diamond saw blade (50 microns thin) cuts the wafer into small dice

**Packaging**

**Overview & Lead frames**
- lead frames – stamped or etched strips of metal sheets

**process steps to built a QFP**
- stamping or etching a lead frame
- die bonding: gluing the chip to the lead frame
- wire bonding: connecting the pads on the die and the pads on the lead frame
- mold everything except the outer leads
- cutting and bending the leads to gullwing form
Packaging

- The thin gold (99.9999% pure and thinner than a human hair) wire is fed through a capillary.
- With the help of ultrasonic excitation the ball is bonded to the first pad.
- The capillary moves to the second pad, where it forms a wedge and cuts the wire in a single step.

Wire Bonding

Packaged Device Test

- Extensive testing of functionality:
  - functional test
  - parametric test
  - IDDQ-test
  - stuck at 1/0
  - serial scan based test
Clean room

Laminar Flow

main function: keep the air clean of particles

Clean room classifications and applications

Main function of clean rooms is control of particle contamination. Requires control of air flow, water and chemical filtrations, human protocol, and operational procedures.

Clean room

Classification

Class: number of particles of size larger than 0.5 um per cubic foot (ft³)

<table>
<thead>
<tr>
<th>Class</th>
<th># 0.5 um particles per ft³</th>
<th># 5.0 um particles per ft³</th>
<th>air changes per hour</th>
<th>ceiling filter coverage (%)</th>
<th>air velocity (fpm)</th>
<th>max. vibration (µin/s)</th>
<th>RH tolerance</th>
<th>approx. capital cost per ft³</th>
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<tbody>
<tr>
<td>office</td>
<td>0.1</td>
<td>10</td>
<td>12-18</td>
<td>10</td>
<td>5</td>
<td>60</td>
<td>5-10%</td>
<td>$10</td>
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<tr>
<td>10,000</td>
<td>10,000</td>
<td>65</td>
<td>15-30</td>
<td>10</td>
<td>10</td>
<td>±10°F</td>
<td>±5%</td>
<td>$200-250</td>
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<tr>
<td>1,000</td>
<td>1,000</td>
<td>0.5</td>
<td>150-300</td>
<td>50</td>
<td>30-60</td>
<td>±2°F</td>
<td>±5%</td>
<td>$550-1,000</td>
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<tr>
<td>100</td>
<td>10</td>
<td>0.05</td>
<td>400-540</td>
<td>80-100</td>
<td>75-90</td>
<td>±1°F</td>
<td>±5%</td>
<td>$1,200</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0.005</td>
<td>800-1,100</td>
<td>100</td>
<td>75-100</td>
<td>±0.3°F</td>
<td>±5%</td>
<td>$3,500</td>
</tr>
</tbody>
</table>

Characteristics:
- temperature controlled to 68-72°F
- humidity controlled to 40-45% RH
- room is held at positive pressure
- doors open inward

Clean room

particles in the air

- in a city: 15 million - 100 million particles per ft³
- in the mountains: up to 10 million particles per ft³
- in a clean room for integrated circuits: 1 - 100 particles per ft³
Clean room

<table>
<thead>
<tr>
<th>motion</th>
<th>emission of particles $&gt;0.5 \mu m$ per minute</th>
</tr>
</thead>
<tbody>
<tr>
<td>street clothes</td>
<td>clean room clothes</td>
</tr>
<tr>
<td>sit without head motion</td>
<td>$3 \times 10^5$</td>
</tr>
<tr>
<td>head motion</td>
<td>$6 \times 10^5$</td>
</tr>
<tr>
<td>slow motion of the body</td>
<td>$10^6$</td>
</tr>
<tr>
<td>slow walking</td>
<td>$3 \times 10^6$</td>
</tr>
<tr>
<td>fast walking</td>
<td>$6 \times 10^6$</td>
</tr>
</tbody>
</table>

Conclusion

Clean Room Dos And Don’ts

**Dos:**
- Change gloves whenever they get dirty or torn
- Use a fresh pair of gloves whenever handling wafers
- Wipe down wafer handling areas with isopropinol
- Use clean room paper and dust-free ball point pens

**Don’ts:**
- Touch your face or skin with gloves
- Touch building hardware, oily machinery, or wafer loading areas
- Lean on equipment
- Wear cosmetics, powders, or cologne
- Wear anything on fingers - no rings and bracelets
- Use paper, pencils or markers that leave dust or lint

Thank you for your attention!