

# Register Files

## Lecture 30

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Mon, Nov 11, 2019

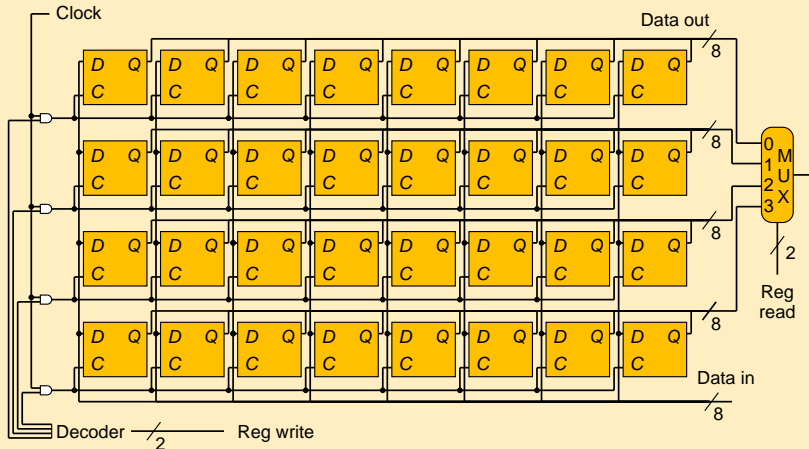
- 1 Register Files
- 2 A Single-Port Register File
- 3 A Dual-Port Register File
- 4 Assignment

# Outline

- 1 Register Files
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# A Register File

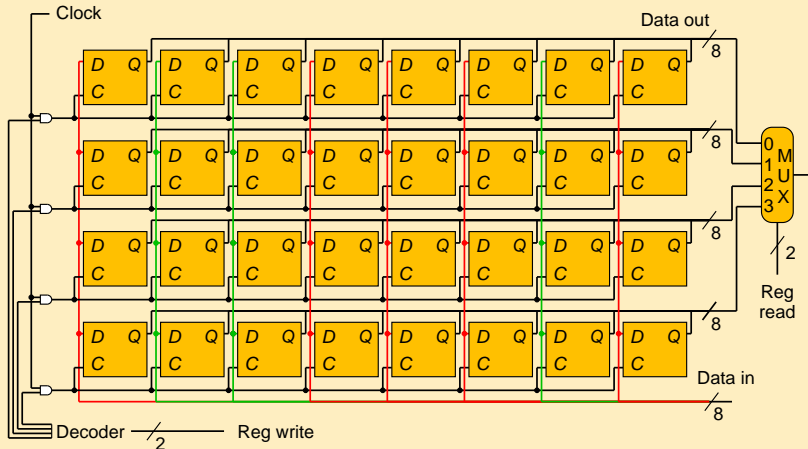
## Register File



A register file of 4 8-bit registers

# A Register File

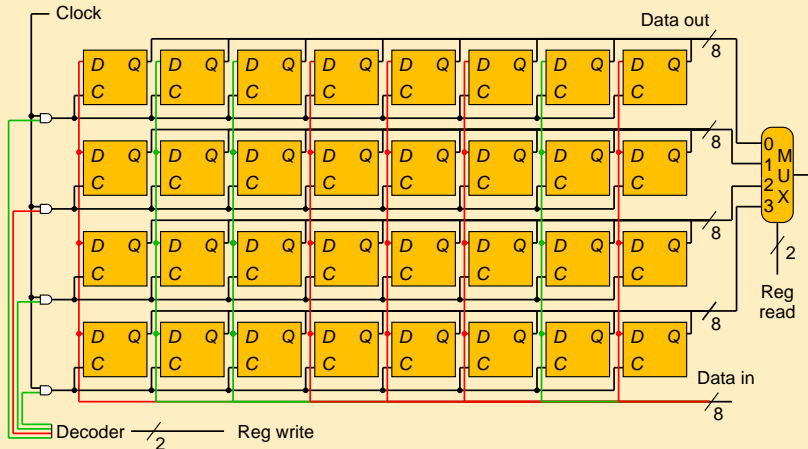
## Register File



Data in = 10011101

# A Register File

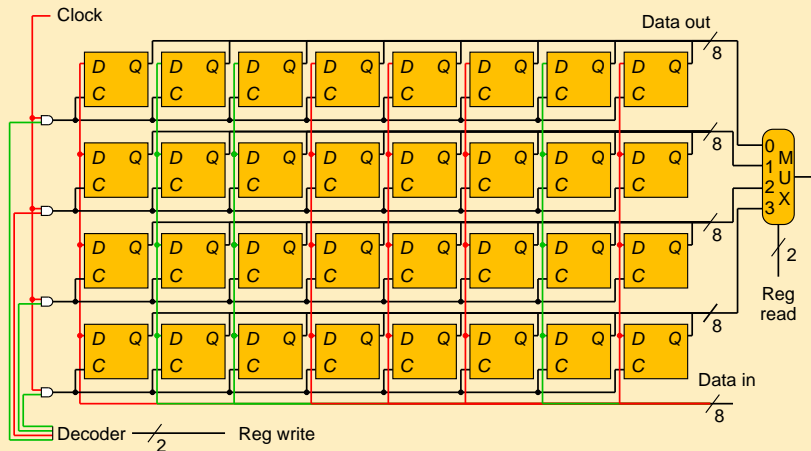
## Register File



Write register = 1

# A Register File

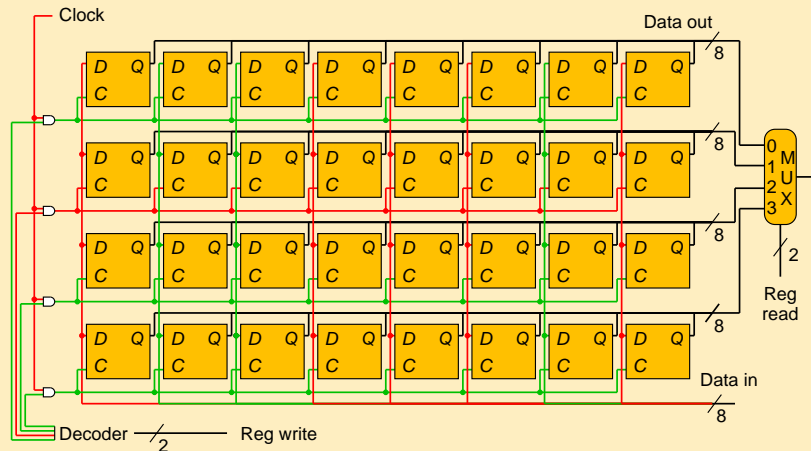
## Register File



Rising edge of clock

# A Register File

## Register File

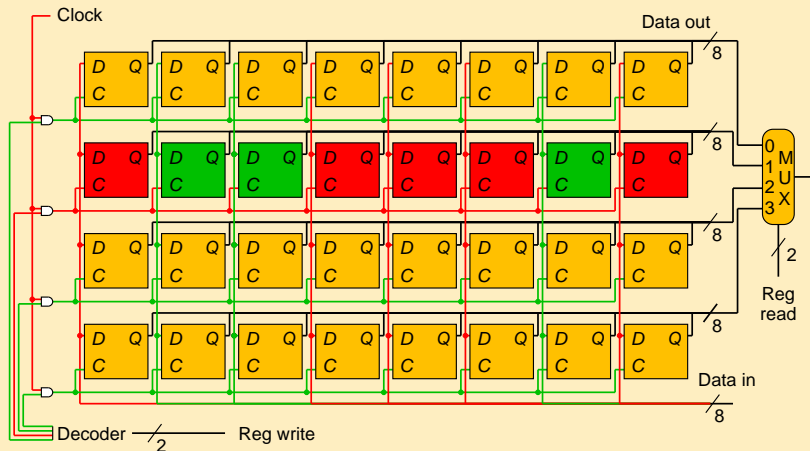


Latches on Register 1 are opened



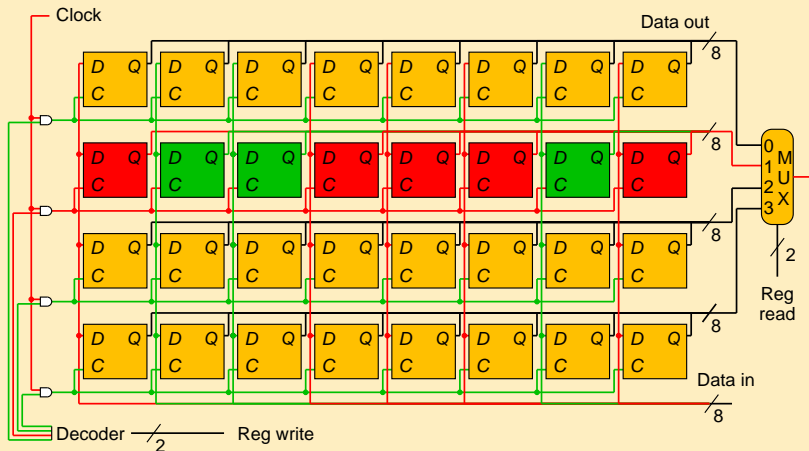
# A Register File

## Register File



# A Register File

## Register File



10011101 is available for reading

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# A Single-Port Register File

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  - Six inputs:

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    - The clock (clk).
    - The clear signal (clr).

# A Single-Port Register File

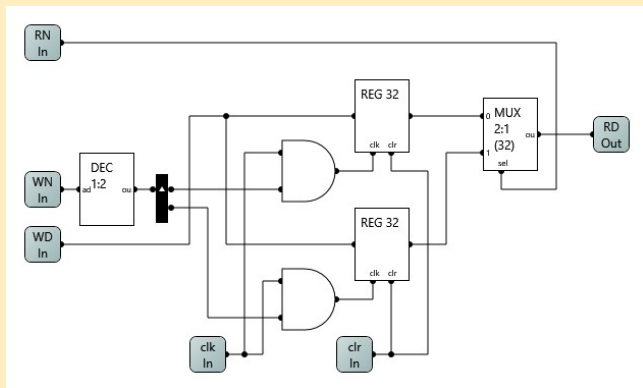
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    - The register to write to (WN).
    - The data to write (WD).
    - The whether-to-write signal (Reg Wrt).
    - The clock (clk).
    - The clear signal (clr).
  - One output:

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    - The register to write to (WN).
    - The data to write (WD).
    - The whether-to-write signal (Reg Wrt).
    - The clock (clk).
    - The clear signal (clr).
  - One output:
    - The value read from the register (RD).

# Single-Port Register Files

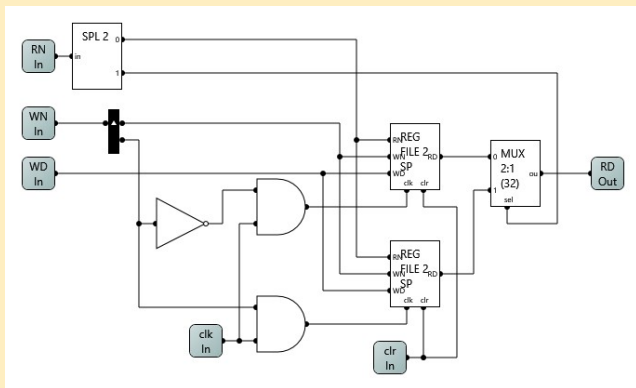
## Single-Port Register Files



Single-port 2-register file

# Single-Port Register Files

## Single-Port Register Files



Single-port 4-register file

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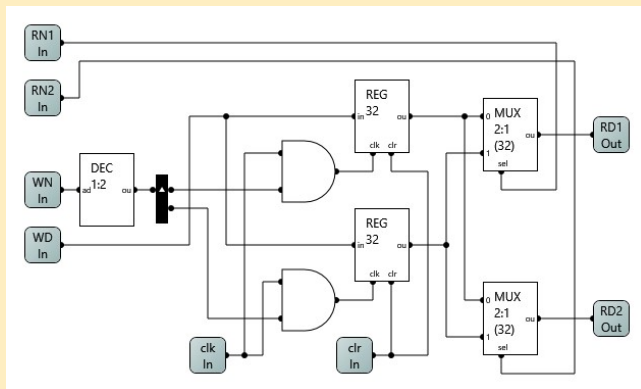
# A Dual-Port Register File

- A dual-port register file of 32 registers has one additional input (second register number) and one additional output (the value of the second register).
- The register numbers are now labeled RN1 and RN2.
- The values read are now labeled RD1 and RD2.



# Dual-Port Register Files

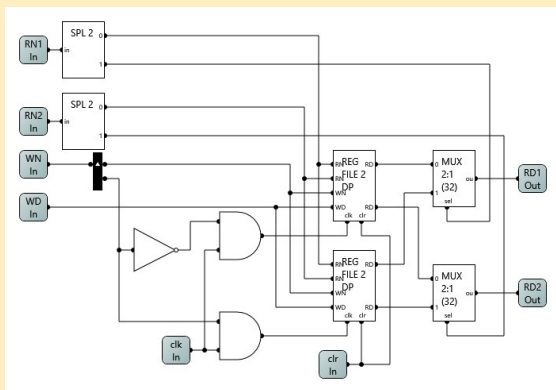
## Dual-Port Register Files



Dual-port 2-register file

# Dual-Port Register Files

## Dual-Port Register Files



Dual-port 4-register file



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# Assignment

## Assignment

- Read Section C.8.